Application for United States Letters Patent

for

Analog Voltage Distribution on a Die using Switched Capacitors

by

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Field

[0001] The invention relates to analog circuits, and more particularly, to switched capacitor circuits.

Background

[0002] Integrated circuits often contain analog functional unit blocks (FUB) that require one or more reference voltages. For example, in Fig. 1, die **102** comprises a microprocessor with many sub-blocks, such as, for example, phase-locked loop **116**, voltage regulator **118**, and interconnect driver **120**. Some of these FUBs allow die **102** to communicate with other integrated circuits, such as off-die cache **104** and higher memory hierarchy levels, such as system memory **108** accessed via host bus **110** and chipset **112**. The reference voltages provided to these various FUBs are often used to set some circuit property, such as, for example, amplifier bias, PLL frequency, or the output voltage of a voltage regulator. The reference voltage should be stable with respect to low and high frequency noise coupled through the semiconductor substrate of die **102**, interconnects, or power supply **114**. Otherwise, the performance of various FUBs may be degraded. For example, the output voltage of a voltage regulator may fluctuate if the reference voltage is not stable.

[0003] Bandgap circuits have been used to generate local reference voltages. However, a bandgap circuit makes use of an amplifier, which may add an offset as well as high frequency power supply noise to the reference voltage. Bandgap circuits at different locations on a die may not provide identical reference voltages due to variations in offset and noise power. A single bandgap circuit may be used to distribute a reference voltage as a single ended signal to different locations on a die. However, a single ended signal is not tolerant to noise coupled through a power supply or the substrate, for example. As a result, differential signaling is often preferred to single-ended signaling. A receiving FUB may utilize a received differential signal directly, or translate the differential voltage into a single-ended voltage referenced to a local ground or local V_{CC}.

[0004] Ideally, common-mode noise in a differential signal may be cancelled by forming the difference of the differential signal to arrive at a single-ended signal. An example of a differencing (or subtracting) circuit is shown in Fig. 2. A differential signal is provided at input ports **202** and **204**. Resistors **206** are designed to have the same

resistance, and the voltage at output port **208** is referenced to ground **210** and is ideally the difference of the voltages at input ports **202** and **204**. Common-mode noise at input ports **202** and **204** is ideally subtracted out. However, in practice there is a matching error in resistors **206**, and their resistance (for well resistors, for example) may be temperature and voltage dependent. Furthermore, there may be an offset and high frequency noise coupling due to amplifier **212**. A low-pass RC filter may be used to filter out high frequency power noise, but due to large MOS gate leakage in present day process technology, it has become difficult to implement an area efficient RC filter with a time constant larger than about 1 nanosecond. There is consequently a need for a noise tolerant voltage distribution technique for present day process technology.

Brief Description of the Drawings

[0005] Fig. 1 depicts a portion of a prior art computer system.

[0006] Fig. 2 depicts a prior art circuit for providing the difference of an input differential voltage signal.

[0007] Fig. 3 depicts an embodiment of the present invention.

[0008] Fig. 4 depicts a circuit for the switched capacitor transformer in the embodiment of Fig. 3.

[0009] Fig. 5a depicts a circuit for the clock generator in the embodiment of Fig. 3.

[0010] Fig. 5b depicts a cycle of operation for the clock generator of Fig. 5a.

[0011] Fig. 6 depicts how two switched capacitor transformers of the type shown in Fig. 4 may be utilized to reduce voltage ripple.

[0012] Fig. 7 depicts another embodiment of the present invention utilizing more than one switched capacitor transformer for providing reference voltage to more than one functional unit block.

Description of Embodiments

[0013] Fig. 3 is a high-level depiction of a system employing an embodiment of the present invention. FUB1 **302** is a functional unit block generating a reference voltage. This reference voltage is provided at input ports **304** and **306** of switched capacitor transformer **308**. Switched capacitor transformer **308** provides a local reference voltage at output ports **310** and **312**. This local reference voltage is utilized by other functional unit

blocks, such as FUB2 **314**, connected to switched capacitor transformer **308** via interconnects **316** and **318**. The embodiment of switched capacitor transformer **308** in Fig. 3 makes use of four clock signals, $\phi_i, i = 1,\ldots,4$, generated by clock unit **320**.

[0014] Differential signaling is employed, where the reference voltage at input ports **304** and **306** is the voltage potential difference between input ports **304** and **306**, and the local reference voltage at output ports **310** and **312** is the voltage potential difference between output ports **310** and **312**. With proper signal routing, noise coupled by interconnects **316** and **318** (or the substrate, not shown) appears as common mode noise and should marginally affect the differential signal (voltage potential difference) on interconnects **316** and **318**. One of the interconnects may be connected to the local ground of FUB2 **314**, but this is not a requirement.

[0015] An embodiment of switched capacitor transformer **308** at the circuit-level is provided in Fig. 4. In some embodiments, capacitors **402** and **404** may not be present. The transistors in Fig. 4 are switched so that there is a first portion of a cycle of operation for which transistors **406** and **408** are both ON to couple capacitor **414** to input ports **416** and **418**, and transistors **410** and **412** are both OFF to isolate capacitor **414** from output ports **420** and **422**; and there is a second portion of a cycle of operation for which transistors **410** and **412** are both ON to couple capacitor **414** to output ports **420** and **422**, and transistors **4106** and **408** are both OFF to isolate capacitor **414** from input ports **416** and **418**. This switching is such that transistors **406** and **410** are not both ON, and transistors **408** and **412** are not both ON.

[0016] During the first portion of a cycle of operation, capacitor **414** develops a potential difference equal to (or more precisely, approximately equal to) the potential difference of input ports **416** and **418**, and during the second portion of a cycle of operation capacitor **414** "transfers" this potential difference to output ports **420** and **422**. In this way, the switched capacitor transformer mitigates low and high frequency power supply noise coupling by acting as a "floating power supply", which may, for example, be referenced to a local ground at the receiving end (FUB2 **314**).

[0017] A circuit for generating the clock signals is provided in Fig. 5a, with a timing diagram of the generated clock signals shown in Fig. 5b. In Fig. 5a, the delay of NAND gates **502** is denoted as T_0, the delay of delay elements **504** is denoted as T_1, and

the delay of delay elements **506** is denoted as T_2. Delay elements **502** and **504** are non-inverting delay elements, and may be implemented by cascading an even number of CMOS inverters. Inspection of the circuit in Fig. 5a yields the clock signals for one cycle (period) are indicated in Fig. 5b, where the clock signals are seen to be periodic with period substantially equal to $4T_0 + 4T_1 + 2T_2$. The portion of the cycle for which both transistors **406** and **408** are ON is the time interval $[t_1, t_2]$ indicated on the time axis of Fig. 5b, and the portion of the cycle for which both transistors **410** and **412** are ON is the time interval $[t_3, t_4]$ indicated on the time axis. These time intervals have the same time duration, indicated as $T_2 + T_1 + T_0$ in Fig. 5b. Note that there are two portions of the cycle for which all the transistors are OFF, which are the time intervals $[t_2, t_3]$ and $[t_4, t_5]$. These time intervals have the same time duration, indicated as $T_1 + T_0$ in Fig. 5b.

[0018] The clock period and the portion of time for which all the transistors are OFF may be adjusted by varying delays T_1 and T_2. For there to be a portion of time for which all transistors are OFF, $T_2 > T_1 + T_0$. Fig. 5b is somewhat idealized because it shows clock signals ϕ_1 and ϕ_2 transitioning at the same time instances, and likewise for clock signals ϕ_3 and ϕ_4. In practice, this need not be the case. Furthermore, in practice, the delays for NAND gates **502** may not be perfectly matched. Likewise for the other delays. However, the delays should be such that the clock signals allow capacitor **414** to be isolated from the input and output ports for some time interval before being coupled to the input ports or the output ports.

[0019] As seen in Fig. 5a, clock signals ϕ_1 and ϕ_2 are inverses of each other. Likewise for clock signals ϕ_3 and ϕ_4. However, if all the transistors in the switched capacitor transformer where to have the same type of majority carriers (e.g., both are nMOSFETs), then clock signals ϕ_2 and ϕ_4 may be taken, respectively, as ϕ_1 and ϕ_3, so that only two clock signals need to be generated. Clearly, various embodiments may be realized depending upon the type of transistors used in the switched capacitor transformer. However, for coupling an input voltage close to V_{CC}, it is preferable to use a pMOSFET because a nMOSFET does not efficiently couple voltages close to or larger than $V_{CC} - V_T$, where V_{CC} is the supply voltage as well as the applied gate voltage to

switch the nMOSFET ON, and V_{TN} is the threshold voltage of the nMOSFET. Likewise, a nMOSFET is preferred for coupling an input voltage close to ground (V_{SS}) because a pMOSFET does not efficiently couple voltages close to or lower than $V_{SS}-V_{TP}$, where V_{TP} is the threshold voltage of the pMOSFET (which is negative for enhancement mode devices). This is the reason why in the embodiment of Fig. 4, it is preferable that transistors **406** and **410** are pMOSFETs and that transistors **408** and **412** are nMOSFETs.

[0020] In practice, the voltage difference between output ports **420** and **422** is not identical to the voltage difference between input ports **416** and **418**. For example, if output ports **420** and **422** are loaded so that a DC current is drawn, then some of the stored charge on capacitor **414** will be drawn by the load and the output differential voltage will not be an identical to the input differential voltage. At low clock frequency, capacitor **404** may help filter out variations in the output differential voltage. Capacitor **402** may be used to reduce noise that may be injected back to the reference distribution network (FUB1 **302**). When a relatively large DC voltage offset is expected between output port **422** and input port **418**, and output port **422** is connected to local ground, then care should be taken to minimize the parasitic capacitance between node **424** and substrate or other signal lines. The parasitic capacitance of node **426** is not as critical. Minimizing parasitic capacitance may be accomplished by using small-sized transistors and by careful layout of capacitor **414**.

[0021] Further reduction in the variation in the output differential voltage due to switching capacitor **414** among the input and output ports may be realized by utilizing two switching capacitor transformers in parallel so that when the switched capacitor of one transformer is coupled to the input ports the switched capacitor of the other transformer is coupled to the output ports. For example, consider the two switched capacitor transformers in Fig. 6. Both SC1 and SC2 have the same structure, but the connections to the clock signals are as indicated in Fig. 6. When the switched capacitor of SC1 is coupled to input ports **602** and **604**, the switched capacitor of SC2 is coupled to output ports **606** and **608**. Similarly, when the switched capacitor of SC1 is coupled to output ports **606** and **608**, the switched capacitor of SC2 is coupled to input ports **602** and **604**.

[0022] If a reference voltage is to be distributed to more than one FUB, then more than one switched capacitor transformer may be used. Fig. 7 provides one such example, where a single differential reference signal is provided to FUB1, FUB2, and FUB3. Each of FUB1, FUB2, and FUB3 may use different power supplies, or some or all may be powered from the same power supply. Also, some of the receiving FUBs may reference their respective received differential signals with respect to local V_{CC}, and some or all of the receiving FUBs may reference the received differential signals with respect to local ground.

[0023] Various modifications may be made to the disclosed embodiments without departing from the scope of the invention as claimed below. For example, it is to be appreciated that the transistors in the embodiment of Fig. 4 act as switches. Other embodiments may be realized by utilizing different switching elements. For example, a so-called complementary switch may be used, comprising a pMOSFET and a nMOSFET in parallel, where the clock signal applied to one of the gates of the complementary switch is the inverse of the clock signal applied to the other gate of the complementary switch. With this in mind, the term "switch" is used in the claims, which may include one or more transistors to operate as a switch. Furthermore, it is to be understood in these letters patent that the phrase "A is connected to B" means that A and B are directly connected to each other, for example, by way of an interconnect, such as metal or polysilicon. This is to be distinguished from the phrase "A is coupled to B", which means that the connection between A and B may not be direct. That is, there may be an active passive element between A and B, or there may be an active device that couples A to B when ON.